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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,003	03/22/2004	Benedict C. Lau	RB1-004USC2	2815

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LEE & HAYES, PLLC
421 W. RIVERSIDE AVE, STE 500
SPOKANE, WA 99201

EXAMINER

WELLS, KENNETH B

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/807,003

Applicant(s)

LAU ET AL.

Examiner

Kenneth B. Wells

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-58 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21-58 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

Art Unit: 2816

DETAILED ACTION

1. Applicant's amendment filed on 11/1/04 has been received and entered in the case.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Specification

3. The disclosure is objected to because of the following informalities: on page 1 of the specification, applicant needs to update the status of the cited copending application 10/158,505 (it has now issued as USP 6,731,148). Appropriate correction is required.

Claim Objections

4. Claim 58 is objected to because of the following informalities: it is incorrect to recite "data transfer" of the first and second signals in claim 58 because these signals are clocks in applicant's invention, not data. Appropriate correction is required.

Art Unit: 2816

Claim Rejections - 35 USC § 102

5. Claims 21-24, 26-30, 32, 35 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's admitted prior art Figs. 1-3.

As to claims 21 and 28, the recited RAM is inside block 104, 106 or 108 (see page 2, lines 3-5 of the instant specification); the recited first and second signal lines are lines 112a and 112b, respectively (see instant Fig. 1); the recited memory controller is element 102 (see instant Fig. 1); the recited DLL is circuit 150 (see instant Fig. 3); the recited first signal is the signal carried on line 112b (i.e. from memory controller 102 to memory storage modules 104, 106, 108); and the recited second signal is the signal carried on line 112a (i.e., from clock generator 120 to memory controller 102).

As to claim 22, the recited driver reads on circuit 170 (see instant Fig. 3).

As to claim 23, note the paragraph bridging pages 2-3 of the instant specification.

As to claim 24, the recited first delay element reads on any of the delay elements within block 154 or block 156 (within the feedback path of DLL 150) and the recited reference clock reads on the (unillustrated) reference

Art Unit: 2816

input to phase detector 164 that is used for determining the necessary phase shift between R-CLK and the second signal (i.e., BUS CLK).

As to claim 26, the recited clock generator reads on clock element 120 (see instant Fig. 1).

As to claim 27, note the page 2, lines 14-15 of the instant specification.

As to claim 29, the recited phase detector reads on circuit 164 (see instant Fig. 3).

As to claim 30, the term "zero phase detector" is broadly interpreted to mean a phase detector with an output that goes to zero when its two inputs have zero phase difference between them (a definition conventionally used in the prior art).

As to claim 32, the 180 degree phase shift of the BUS CLK signal (the recited "second signal" of the instant claims) is inherent within the loop block 156, i.e., cascaded delay elements that shift the phase of the second signal (which is also output from block 154) by a plurality of incremental amounts, including 180 degrees.

As to claims 35 and 36, the recited receive clock reads on clock signal R-CLK output from buffer 158.

Art Unit: 2816.

6. Claims 37, 40, 41, 44-46, 48, 51 and 52 are rejected under 35 U.S.C. 102(e) as being anticipated by Coddington et al.

As to claim 37, note Fig. 2, where the recited "first signal" reads on the clock at terminal 94; the recited "single DLL" reads on circuit 70; the recited "reference signal" reads on the clock at terminal 52; the recited "second delay element" reads on either delay element 90 or 91; the recited "second signal" reads on the feedback clock at terminal 97; and the recited "first delay element" reads on element 92. The functional limitations of claims 40, 41, 44-46, 48, 51 and 52 are all deemed to be inherent in the operation of Fig. 2 of Coddington et al.

Claim Rejections - 35 USC § 103

7. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art Figs. 1-3 in view of either Erickson or Self et al.

Though not disclosed by applicant's admitted prior art, the sampling of data on both the rising and falling edges of the second signal (i.e., BUS CLK) would have been obvious to those having ordinary skill in the art because it is well-known in the art to do this, as taught by the

Art Unit: 2816

two secondary references, for the well-known benefits of (1) more reliable timing, see Erickson at column 3, last paragraph, and (2) achieving higher data transfer rates, see the disclosure by Self et al. Thus, claim 34 does not patentably distinguish over applicant's admitted prior art Figs. 1-3.

8. Claims 38, 39, 53-56 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coddington et al in view of applicant's admitted prior art Figs. 1-3.

The details of claims 38 and 39, though not disclosed by Coddington et al, are all taught in applicant's discussion of instant Figs. 1-3. It would have been obvious to those having ordinary skill in the art to use the DLL system of Coddington et al with the conventional data transfer circuitry disclosed by applicant in order to obtain the benefits taught by Coddington et al, i.e., improved locking reliability of the output clocks supplied to external circuits 114 and 116 relative to the system clock at terminal 52.

As to claim 53, the electronic data store and controller have been discussed above regarding instant

Art Unit: 2816

Figs. 1-3, and the recited limitations of the DLL are discussed above with regard to Fig. 2 of Coddington et al. The functional limitations of claims 54-56 and 58 are all deemed to be inherent in the operation of Fig. 2 of Coddington et al.

9. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coddington et al in view of either Erickson or Self et al.

Note paragraph six above as to the obviousness of sampling of data on both the rising and falling edges of a clock signal.

Double Patenting

10. Claims 21-58 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 6,731,148 and claim 7 of U.S. Patent No. 6,469,555. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant claims are all anticipated by the inventions claimed in the previous two patents.

Art Unit: 2816

Allowable Subject Matter

11. Claims 25, 31, 33, 42, 43, 47, 49 and 57 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the

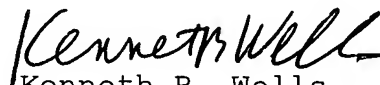
Art Unit: 2816

statutory period for reply expire later than SIX MONTHS
from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Kenneth B. Wells
Primary Examiner
Art Unit 2816

December 10, 2004